

LOW OVERHEAD READ BUFFER

ABSTRACT OF THE DISCLOSURE

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A memory controller includes logic for requesting a read operation from memory and logic for generating an address for the read operation. The memory controller also includes logic for storing both, data associated with the address and data associated with a consecutive address in temporary storage. Logic for determining if a request for data 10 associated with a next read operation is for the data associated with the consecutive address in the temporary storage is also provided. A method for optimizing memory bandwidth, a device and an integrated circuit are also provided.